Amendments to the Specification:

At page 3, line 25 replace the paragraph with the following;

A video input selector for a multimedia display device is depicted in simplified form in FIGURE 1. FIGURE 1 includes selector 5, which forms part of integrated circuit 6, allows user selection by means of I^2C control bus, between a composite encoded video signal Vc, for example, a NTSC or PAL encoded signal, and a luminance signal component Yc input from a signal source which provides separate luminance and chrominance signal components, for example S-Video, coupled via connector J2. Switch 4 couples the composite encoded video signal, (NTSC or PAL), to a comb filter within IC 6 that removes color subcarrier signals and provides separation of luminance and chrominance (chroma) components from the composite signal Vc. Switch 3 selects the luminance video component Yc input from an S-video signal input at connector J2. Since the luminance component Yc represents a separated or derived luminance signal it does not require comb filtering to remove any color subcarrier signal, thus it is coupled within IC 6 to a point following comb filter processing. Integrated circuit 6, for example an F2PIP/Comb filter, generates both a chrominance signal (chroma) and a luminance signal (Yo) responsive to selection controlled by the I^2C control bus. Signal Yo is coupled via a wire conductor to provide an input signal that is coupled via printed conductor track 24A to a series connected resistor R3 and via printed conductor track 24B to selector switch ~~4~~ S1A of IC 2, for example CMOS type 74HC4053. The chrominance signal, chroma, from block IC 6 is coupled directly to video processor integrated circuit IC 1, for example Toshiba type TA1276, for demodulation to produce color difference signal components. The demodulated color difference signals for example I/Q or R-Y/B-Y are output from video processor IC 1 and coupled to selector ~~switch S2~~ switches S2A1 and S2A2 of IC 3 which facilitates selection between demodulated color difference signals and component input color difference signals, Pr/Pb from an external signal source.

At page 5, line 7 replace the paragraph with the following;

Luminance signal Yext is AC coupled by capacitor C3 and supplied as signal Yext1 to selector switch S2B of integrated circuit IC 3 for coupling to video processor IC 1 as signal Y2in. Similarly signal Yext is AC coupled by capacitor C4

and supplied as signal Yext2 to switch ~~S1~~ S1B of integrated circuit IC 2 for coupling as a synchronizing signal to integrated circuit T4 (not shown).

At page 5, line 12 replace the paragraph with the following;

Stray or parasitic capacitance can exist between printed conductor tracks 22B and 22BB respectively, and track 24B. These stray capacitances are depicted as capacitors Cs1 and Cs2 shown with dashed lines. It can be appreciated that when a luminance signal Yext is present on connector J1, high frequency energy present in signals Yext1 and Yext2 will be coupled via stray capacitors Cs1 and Cs2 to ~~on~~ conductor 24B and consequently luminance signal Yo. Similarly luminance signal Yo will be coupled onto conductor tracks 22B and 22BB. However, this reciprocal cross coupling is avoided because signal Yo is inhibited when viewing external component signals, as will be explained.

At page 6, line 5 replace the paragraph with the following;

Selection between an external component signal and the various internally derived signals is controlled by addressing the various switching elements via the I^2C control bus. Video processor IC 1 receives the I^2C control bus and generates switch control signal ~~1~~ 20 (CTRL 1), which is coupled to switches S1 and S2A/B which provide a series switching function to select between internal and external luminance and color difference signals. In addition control signal ~~1~~ 20 is coupled to an inventive shunt switch shown in block 16 and applied to the base terminal of an NPN transistor Q1 via resistor R5. The base terminal of transistor Q1 is also coupled to ground via resistor R4 thus providing a potential divider for control signal 1. The collector of transistor Q1 is connected to the base terminal of an NPN transistor Q2 and to a power supply, for example +9v, via resistor R3. The emitter terminals of transistors Q1 and Q2 are connected to ground. The collector of transistor Q2 is connected to a pair of capacitors C1 and C2. Capacitor C2 is connected to the junction of capacitor C3, zener diode D1 and an input of switch ~~S2 at~~ S2B via conductor 22B. Similarly capacitor C1 is connected to the junction of capacitor C4, Zener diode D2 and an input of switch S1B at conductor 22BB.

At page 6, line 21 replace the paragraph with the following;

Operation of inventive shunt switch 16 will now be explained. When an external component signal is selected control ~~1, at~~ signal 20, assumes a positive

voltage value of approximately 5 volts or greater, and conversely when the internally derived signals are selected control ~~1~~ signal 20 assumes a low or substantially zero voltage value. Thus with external components selected, the positive voltage of control ~~1~~ signal 20 causes transistor Q1 to turn on and assume a saturated state. With transistor Q1 saturated, transistor Q2 ~~receive~~ receives no base current and is held off with the collector terminal assuming a high impedance. Thus, capacitors C1 and C2 are effectively connected in series between nominally identical, AC coupled signals Yext1 and Yext2 present on conductors 22B and 22BB respectively. As described previously, unwanted cross coupling of internal signal Yo via stray capacitors Cs1 and Cs2 into external luminance signals Yext1/Yext2 is prevented within block 5 of IC6.